

MK1518C LDMOS TRANSISTOR

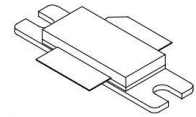
Document Number: MK1518C
Preliminary Datasheet V1.0

180W, 28V High Power RF LDMOS FETs

Description

The MK1518C is a 180-watt high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1.5GHz.

MK1518C



- Typical Performance (On Innogration 1GHz narrow band fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 200$ mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	$\eta_D @ P_{-1}$ (%)
1000 MHz	18	180	65

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 1GHz below high performance amplifier where demands single ended device
- 1300MHz particle accelerator
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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

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Drain-Source Voltage $V_{GS}=0$, $I_{DS}=1.0\text{mA}$	$V_{(BR)DSS}$	65	70		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}$, $I_D = 600\text{ }\mu\text{A}$)	$V_{GS(th)}$	—	1.98	—	V
Gate Quiescent Voltage ($V_{DD} = 28\text{ V}$, $I_D = 200\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.53	—	V
Drain source on state resistance ($V_{DS} = 0.1\text{V}$, $V_{GS} = 10\text{ V}$)	$R_{ds(on)}$		220		$\text{m}\Omega$
Common Source Input Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{ V}$, $f = 1\text{ MHz}$)	C_{ISS}		170		pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{ V}$, $f = 1\text{ MHz}$)	C_{OSS}		70		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{ V}$, $f = 1\text{ MHz}$)	C_{RSS}		3		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 200\text{ mA}$, $f = 1000\text{ MHz}$, CW Signal Measurements.

Power Gain	G_p	—	18	—	dB
Drain Efficiency@P1dB	η_D	—	65	—	%
1 dB Compression Point	$P_{-1\text{dB}}$	—	100	—	W
Input Return Loss	IRL	—	-7	—	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 200\text{ mA}$, $f = 1000\text{ MHz}$

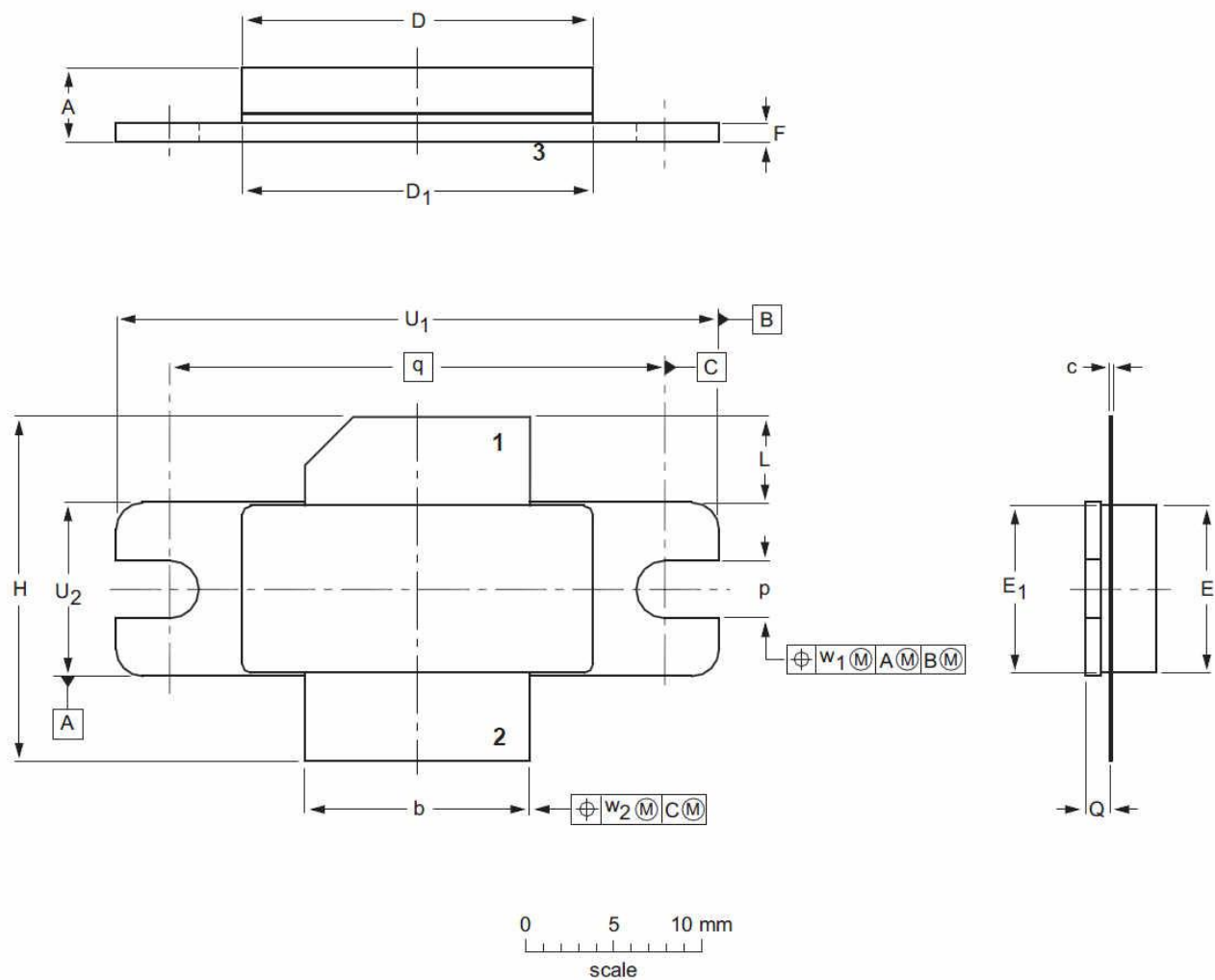
VSWR 10:1 at 180W CW Output Power	No Device Degradation
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Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	p	Q	q	U ₁	U ₂	W ₁	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	3.12	1.45	27.94	33.91	9.65	0.25	0.51
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.123	0.057	1.100	1.335	0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/8/2	Rev 1.0	Preliminary Datasheet Creation

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